substrate, wherein the circuitry is positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer.

43. The integrated circuit of claim 42 wherein the substrate is a silicon substrate.

44, The integrated circuit of claim 42 wherein the I/O buffer is an output buffer.

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45. The integrated circuit of claim 42 wherein the I/O buffer is an input buffer.

46. The integrated circuit of claim 42 wherein the I/O buffer is a complementary output buffer.

47. The integrated circuit of claim 42 wherein the circuitry is CMOS circuitry.

48. The integrated circuit of claim 42 wherein the circuitry is BiCMOS circuitry.

49. The integrated circuit of claim 42 wherein the circuitry is an application specific integrated circuit.

50. The integrated circuit of claim 42 wherein the circuitry is digital signal processor.

51. The integrated circuit of claim 42 wherein the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

52. A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

53. A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

54. The semiconductor wafer of claim 53 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

55 An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

C 1 an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

56 An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

57. The circuit of claim 56 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

58. A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

59. A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

60. The method of claim 59 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

61 A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing an electrostatic discharge device; and

providing an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

62 A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing an electrostatic discharge device disposed at least partially beneath said bond pad; and

providing an I/O buffer disposed between said scribe region and said core region.

63. The method of claim 62 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.